

Compound Field Effect Power Transistor

μ PA1520B

N-CHANNEL POWER MOS FET ARRAY SWITCHING USE

DESCRIPTION

The μ PA1520B is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
 $I_{D(DC)} = \pm 2.0$ A
 $R_{DS(on)1} \leq 0.17 \Omega$ MAX. ($V_{GS} = 10$ V, $I_D = 1$ A)
 $R_{DS(on)1} \leq 0.25 \Omega$ MAX. ($V_{GS} = 4$ V, $I_D = 1$ A)
- Low Input Capacitance $C_{iss} = 220$ pF TYP.

ORDERING INFORMATION

Type Number	Package
μ PA1520BH	10 Pin SIP

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS} Note 1	30	V
Gate to Source Voltage	V_{GSS} Note 2	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$ Note 3	± 8.0	A/unit
Total Power Dissipation	P_{T1} Note 4	28	W
Total Power Dissipation	P_{T2} Note 5	3.5	W
Channel Temperature	T_{CH}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes 1. $V_{GS} = 0$

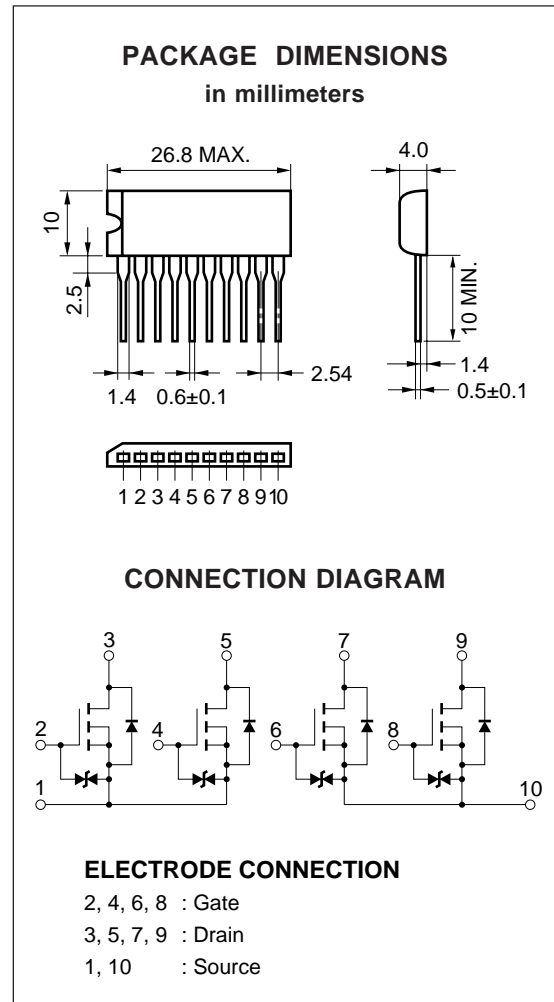
2. $V_{DS} = 0$

3. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

4. 4 circuits, $T_C = 25^\circ\text{C}$

5. 4 circuits, $T_A = 25^\circ\text{C}$

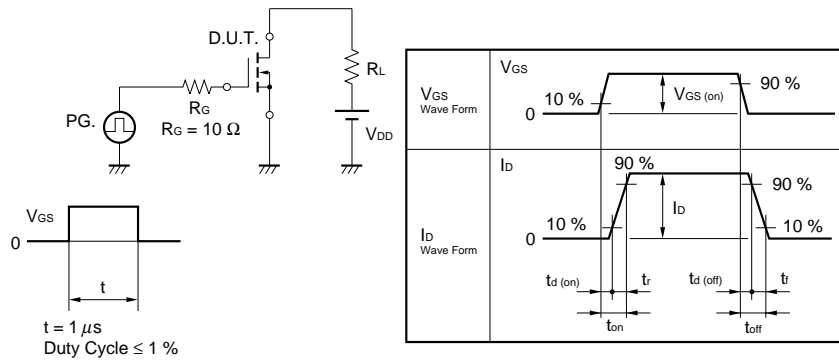
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



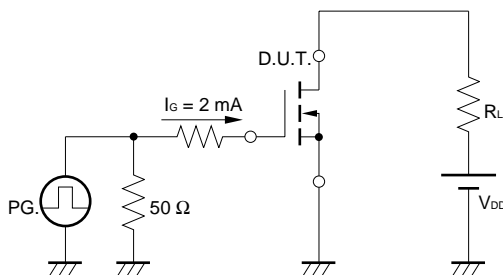
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Gate Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	1.0		2.0	V
Forward Transfer Admittance	Y _{fs}	V _{DS} = 10 V, I _D = 1.0 A	1.0			S
Drain to Source On-State Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 1.0 A		0.10	0.17	Ω
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 1.0 A		0.13	0.25	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0, f = 1.0 MHz		220		pF
Output Capacitance	C _{oss}			220		pF
Reverse Transfer Capacitance	C _{rss}			90		pF
Turn-on Delay Time	t _{d(on)}	I _D = 1.0 A, V _{GS} = 10 V, V _{DD} ≅ 15 V, R _L = 15 Ω		27		ns
Rise Time	t _r			125		ns
Turn-off Delay Time	t _{d(off)}			590		ns
Fall Time	t _f			500		ns
Total Gate Charge	Q _G	V _{GS} = 10 V, I _D = 2.0 A, V _{DD} = 24 V		14		nC
Gate to Source Charge	Q _{GS}			2		nC
Gate to Drain Charge	Q _{GD}			5.5		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 2.0 A, V _{GS} = 0		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 2.0 A, V _{GS} = 0, di/dt = 50 A/μs		640		ns
Reverse Recovery Charge	Q _{rr}			3.4		μC

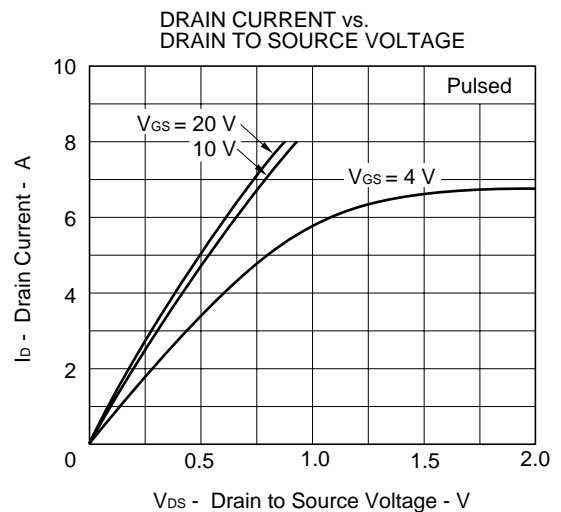
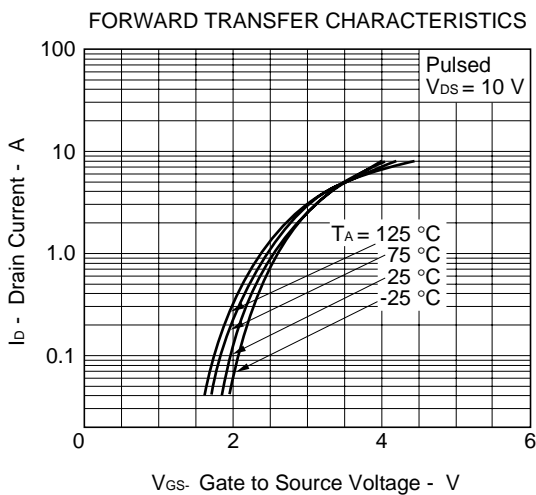
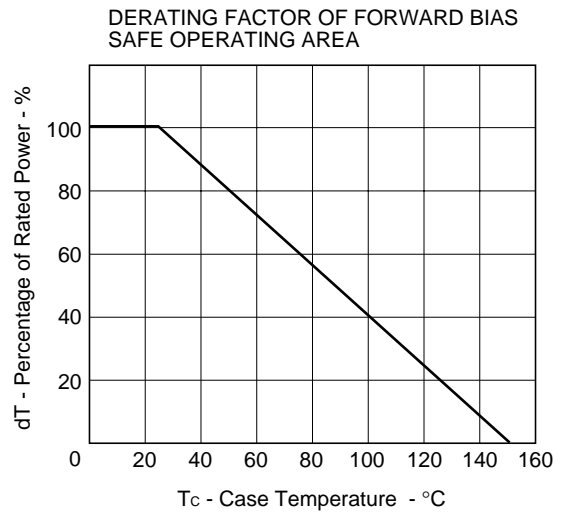
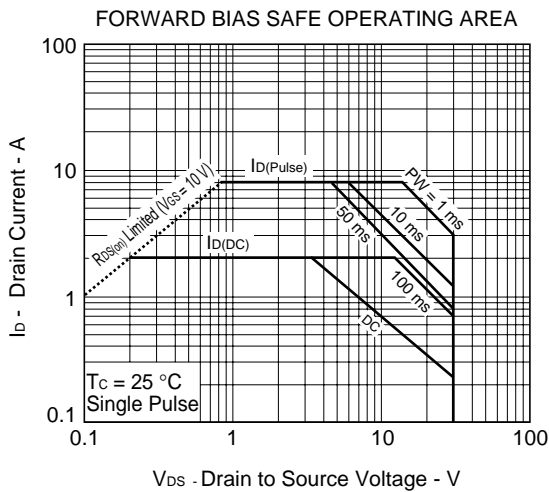
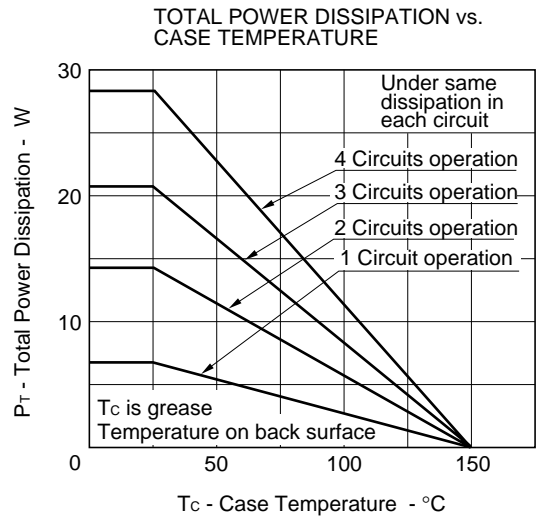
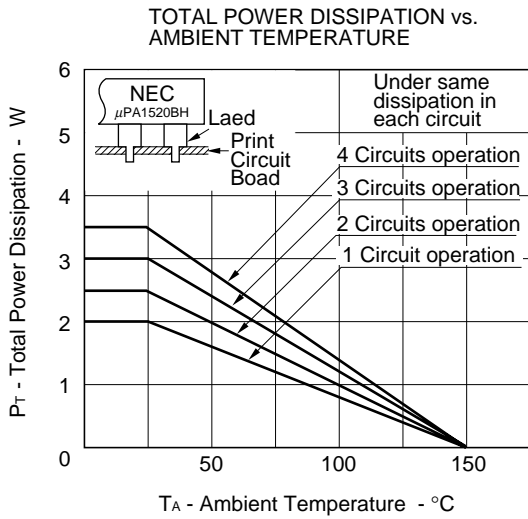
Test Circuit 1 Switching Time



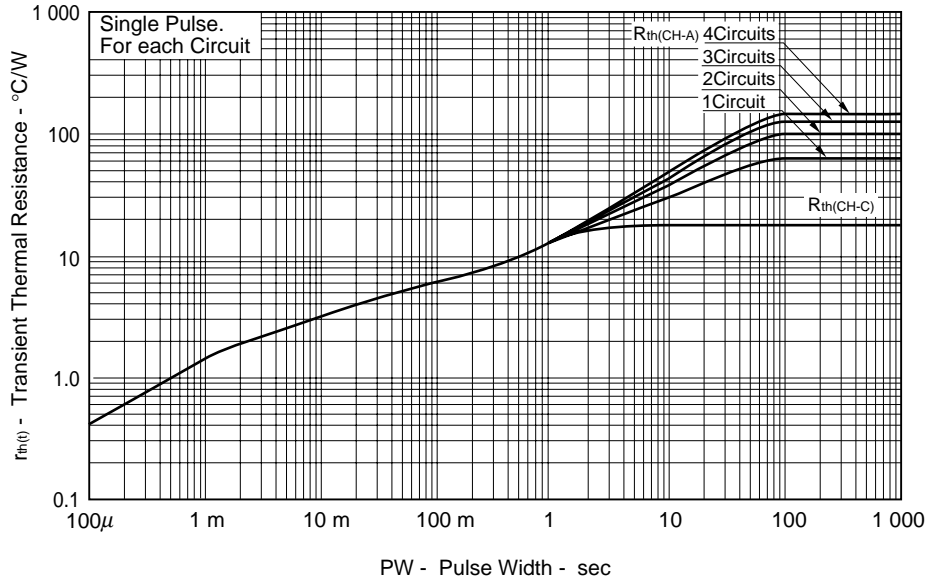
Test Circuit 2 Gate Charge



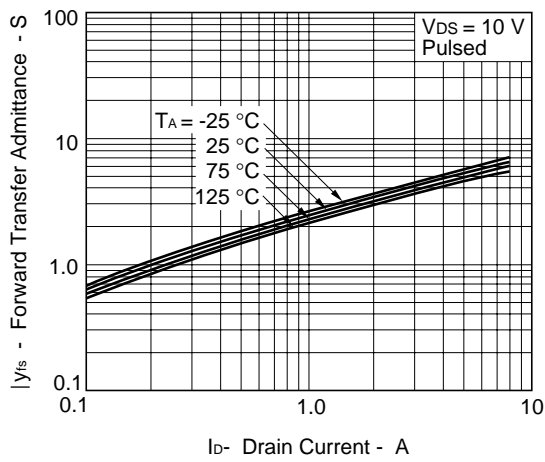
CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$)



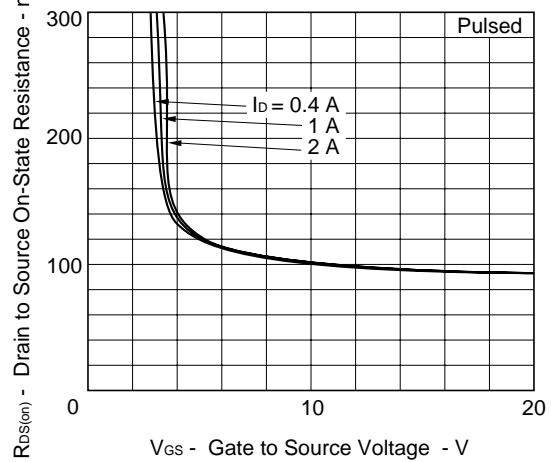
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



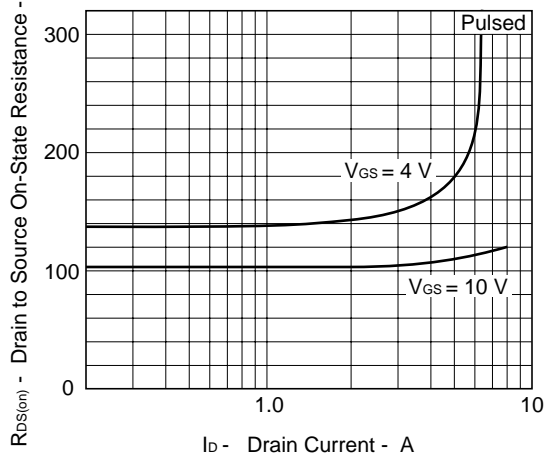
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



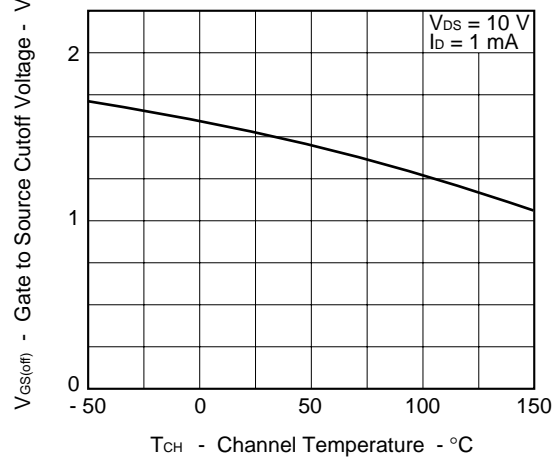
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

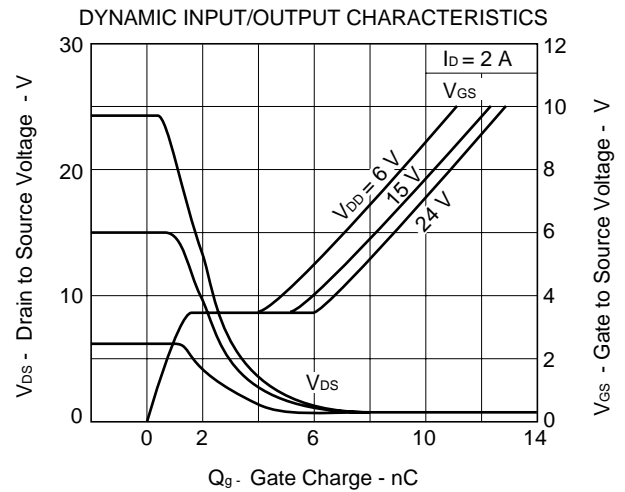
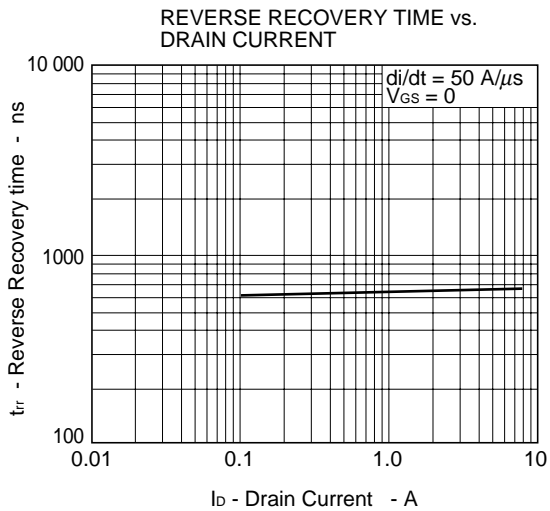
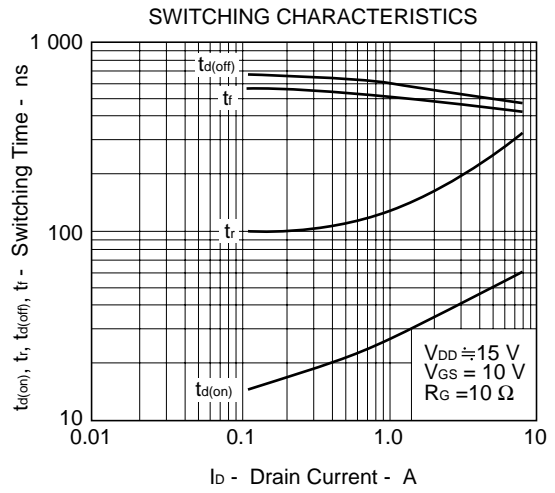
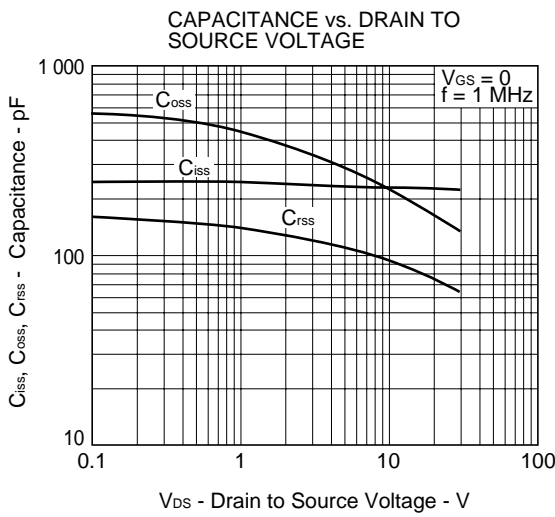
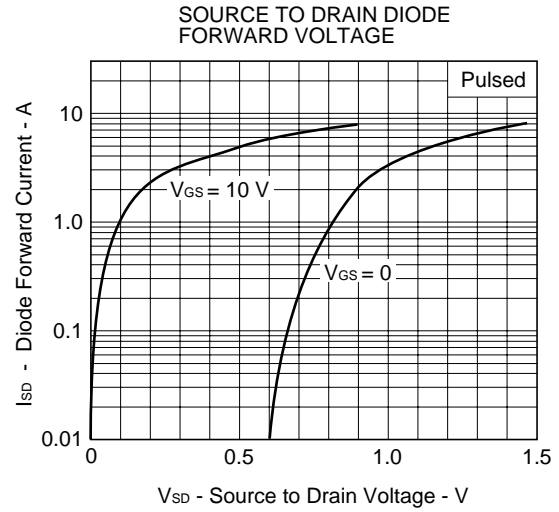
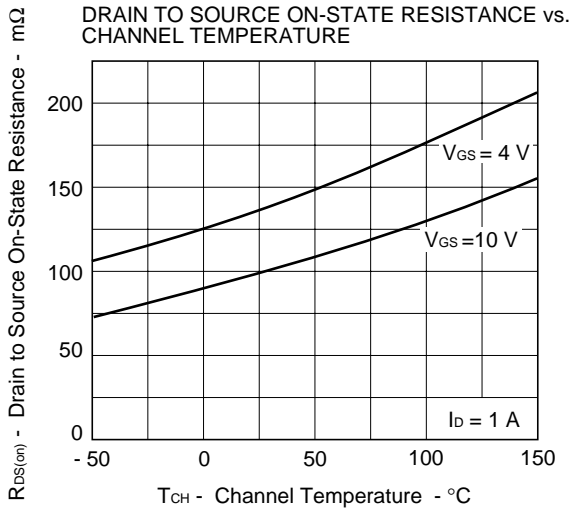


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	IEI-1207
Semiconductor device package manual	IEI-1213
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	MF-1134
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

[MEMO]

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Anti-radioactive design is not implemented in this product.